REMARKS

Claims 5-9 are now present in this application.

The specification and claims 5-9 have been amended, and claims 1-4 have been canceled without prejudice or disclaimer. Reconsideration of the application, as amended, is respectfully requested.

Claims 3 and 9 stand objected to for certain informalities. Because these informalities have been addressed, it is respectfully requested that any objection to the claims now be reconsidered and withdrawn.

Claims 1 and 4-8 stand rejected under 35 USC 103 as being unpatentable over HARDEE, U.S. Patent 5,389,842 in view of IGARASHI, U.S. Patent 4,656,491, or STEUDEL, U.S. Patent 3,712,995. These rejections are respectfully traversed.

Claims 2-3 and 9 stand rejected under 35 USC 103 as being unpatentable over HARDEE, IGARASHI and STEUDEL in further view of KER et al., U.S. Patent 6,072,219. This rejection is respectfully traversed.

In independent claim 5, an ESD protection component is set forth. This component has each of the MOS FETs with a source region of the first conductivity type coupled to a power rail. The prior art utilized by the Examiner fails to disclose such an arrangement.

In the Office Action, the patent the HARDEE et al. is alleged to show this feature. However, in Fig. 2 of this patent, there is only one MOS FET 26 having a source region 24 coupled to a power rail VCCEXT. The source region 44 of the other MOS FET 42 is not coupled to the power rail.

Moreover, in column 5, lines 33-35 of HARDEE, the region 44 is set forth as being coupled by a representative "conductive" line to provide the output signal of the integrated circuit device. Accordingly, HARDEE does not teach that each of the MOS FETs has a source region of the first conductivity type coupled to a power rail. At least for this reason alone, claim 5 should be distinguished from the prior art utilized by the Examiner.

Turning to independent claim 6, an ESD protection component is set forth. It is recited that the first well is coupled to a pad through the extension area. In the prior art utilized by the Examiner, it is alleged that one skilled in the art would find it obvious to connect the pad to the first well through the extension area in order to reduce the contact resistance of the device. In Fig. 2 of HARDEE, however, the first well 22 is not coupled to a pad. Moreover, in the text of col. 5, lines 21-25 of HARDEE, it is set forth that, within region 22, an N+ diffusion or region 32 has been constructed. This region 32 is heavily doped, preferably

arsonic or phosphorous region, that is electrically coupled to receive the voltage VCCP. Accordingly, the well 22 in HARDEE is taught to be coupled to receive a voltage VCCP by heavily doped region 32, but is not coupled to a pad. It would therefore not be obvious to one skilled in the art to connect the pad to the first well, since HARDEE does not teach such a first well connected to the pad. The additional references to IGARASHI or STREUDEL would not overcome this deficiency. There is no suggestion in the prior art utilized by the Examiner to arrive at an ESD protection component as recited in independent claim 6 of the present application.

Turning to independent claim 7, an ESD protection component is recited. In this component, the first doping region is coupled to a pad. It is alleged that HARDEE teaches in Fig. 2 and related text, an ESD protection component which has a first doping area 34 with the first doping region coupled to a pad. However, in Fig. 2 of HARDEE, the doping region 34 is coupled to the drain region 28 rather than the pad. Additionally, in column 5, lines 14-16 of HARDEE, it is set forth that "region 34 is a source electrode of transistor 14 and is connected to N+ region 28 by a representative conductive line". Accordingly, HARDEE would not teach a first

doping region coupled to the pad. The secondary references to IGARASHI and STREUDEL would also fail to show this feature.

In independent claim 8, an ESD protection component is recited, wherein each of the MOS FETs has a drain region of the first conductivity type, coupled to a pad. Again, HARDEE is alleged to teach at least two MOS field effect transistors 26, 42, wherein each of the MOS FETs have a drain region of the first conductivity type coupled to a pad. In Fig. 2 of HARDEE, however, neither drain region 28 nor 44 of the MOS FETs 26 and 42 are coupled to a pad. In the related text in column 5, lines 14-16 and lines 33-35, HARDEE teaches "region 34 is a source electrode of transistor 14 and is connected to N+ region 28 by representative conductive line" and "region 44 is coupled by a representative (conductive) line to provide the output signal of the integrated circuit device". Thus, HARDEE would not teach that each of the MOS FETs has a drain region of the first conductivity type coupled to a pad. The HARDEE reference and the other prior art utilized by the Examiner would fail to show the ESD protection component of claim 8.

In independent claim 9, an ESD protection component is recited. None of the prior art utilized by the Examiner discloses nor suggests two MOS field effect transistors, both having sources coupled to a power supply and the first well and doping are coupled

to a pad. In section 9 of the Office Action, the prior art is alleged to teach this claimed structure. However, as has been previously described, the patent to HARDEE teaches a source region 44 of the MOS FET 42 being coupled to provide the output signal of the integrated circuit device, rather than a power supply, and the first well 22 and doping region 34 respectively being coupled to receive a voltage VCCP and the N+ region 28 rather than the pad. The claimed ESD protection device would neither be suggested nor rendered obvious by any of the prior art utilized by the Examiner.

The HARDEE reference alone, or as modified by IGARASHI, STREUDEL and KER et al. would fail to suggest or render obvious the ESD protection component as recited in the claims of the present application. Accordingly, it is respectfully requested that the 35 USC 103 rejections now be reconsidered and withdrawn.

Because the additional prior art cited by the Examiner has been included merely to show the state of the prior art and has not been utilized to reject the claims, no further comments concerning these documents are considered necessary at this time.

In the event that any outstanding matters remain in this application, the Examiner is invited to contact the undersigned at (703) 205-8000 in the Washington, D.C. area.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), the Applicants respectfully petition for a one (1) month extension of time for filing a response in connection with the present application and the required fee of $110.00 is attached herewith.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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0941-0342P

Attachment: Version with Markings to Show Changes Made

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

A paragraph has been added after the paragraph ending on page 4, line 4.

The paragraph beginning on page 4, line 6, has been amended as follows:

--The present invention can be more fully understood by reading the subsequent detailed description in conjunction with the examples and references made to the accompanying drawings, which are given by way of illustration only, and thus are not limitative of the present invention, and wherein:--

IN THE CLAIMS:

Claims 1-4 have been canceled without prejudice or disclaimer of the subject matter contained therein.

The claims have been amended as follows:

5. (Amended) [The ESD protection circuit as claimed in claim 1,] An ESD protection component, comprising:

at least two MOS field effect transistors (FETs) of a first conductivity type, having two gates and formed in parallel on a first semiconductive layer having a second conductivity type; and

a first well having a first conductivity type, formed on the first semiconductive layer, comprising:

a connecting area, formed between the MOS FETs;

two parallel extension areas, formed perpendicular to the gates of the MOS FETs; and

a first doping area of the second conductivity type, formed in the connecting area;

wherein each of the MOS FETs has a source region of the first conductivity type, coupled to a power rail.

6. (Amended) [The ESD protection circuit as claimed in claim 1,] An ESD protection component, comprising:

at least two MOS field effect transistors (FETs) of a first conductivity type, having two gates and formed in parallel on a first semiconductive layer having a second conductivity type; and

a first well having a first conductivity type, formed on the first semiconductive layer, comprising:

a connecting area, formed between the MOS FETs;

two parallel extension areas, formed perpendicular to the gates of the MOS FETs; and

a first doping area of the second conductivity type, formed in the connecting area;

wherein the first well is coupled to a pad through the extension areas.

7. (Amended) [The ESD protection circuit as claimed in claim 1,] An ESD protection component, comprising:

at least two MOS field effect transistors (FETs) of a first conductivity type, having two gates and formed in parallel on a first semiconductive layer having a second conductivity type; and

a first well having a first conductivity type, formed on the first semiconductive layer, comprising:

a connecting area, formed between the MOS FETs;

two parallel extension areas, formed perpendicular to the gates of the MOS FETs; and

a first doping area of the second conductivity type, formed in the connecting area;

wherein the first doping region is coupled to a pad.

8. (Amended) [The ESD protection circuit as claimed in claim 1,] An ESD protection component, comprising:

at least two MOS field effect transistors (FETs) of a first conductivity type, having two gates and formed in parallel on a first semiconductive layer having a second conductivity type; and

a first well having a first conductivity type, formed on the first semiconductive layer, comprising:

a connecting area, formed between the MOS FETs;

two parallel extension areas, formed perpendicular to the gates of the MOS FETs; and

a first doping area of the second conductivity type, formed in the connecting area;

wherein each of the MOS FETs has a drain region of the first conductivity type, coupled to a pad.

9. (Amended) An ESD protection component, comprising:

at least two MOS field effect transistors (FETs) of a first conductivity type, comprising:

two gates, formed in parallel on a first semiconductive layer having a second conductivity type;

two sources of the first conductivity type, coupled to a power supply; and

two drains of the first conductivity type;

a first well having a first conductivity type, formed on the first semiconductive layer, comprising:

a connecting area, formed between the MOS FETs;

[Two] two parallel extension areas, formed perpendicular to the gates of the MOS FETs; and

a first doping area of the second conductivity type, formed in the connecting area, and coupled to a pad; and

a guard ring of the second conductivity type, formed on the first semiconductive layer, coupled to the power supply;

wherein the [firsPt] first well is coupled to the pad through the extension areas.